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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P8265 Total Pages 3

First Named Inventor or Application Identifier Kevin X. Zhang

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JC530 U.S. PTO
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ADDRESS TO: **Assistant Commissioner for Patents**
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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 28)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 17)

4. X Oath or Declaration (Total Pages 5)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. __ Assignment Papers (cover sheet & documents(s))
9. __ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__ b. Power of Attorney
10. __ English Translation Document (if applicable)
11. __ a. Information Disclosure Statement (IDS)/PTO-1449
__ b. Copies of IDS Citations
12. __ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. __ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. __ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. __ Other: _____

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
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18. **Correspondence Address**
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Attorney Docket No. 42390.P8265 *PATENT*

UNITED STATES PATENT APPLICATION

FOR

SHARED CACHE WORDLINE DECODER FOR REDUNDANT AND REGULAR ADDRESSES

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SHARED CACHE WORDLINE DECODER FOR BOTH REDUNDANT AND REGULAR ADDRESSES

FIELD OF THE INVENTION

This invention relates generally to decoders for memory, and in particular to decoders for high-speed cache memory.

BACKGROUND OF THE INVENTION

A cache is a fast memory for storing copies of frequently accessed data. As processors become faster, cache access time is often a dominating factor in system performance. Conflicting goals face designers of cache memory systems. Smaller caches provide faster access times, but larger caches provide higher hit ratios, thereby reducing penalties associated with accessing slower memory.

Since a current trend in processor design is to devote a substantial proportion of chip area to cache memory, much effort has been invested in improving access times for large caches.

One prior art method shown in, for example, U.S. Patent No. 5,532,947 combines an adder for generating an effective address with a word-line decoder. This combined decoder/adder is shown in Figure 1. Another prior art method shown in, for example, U.S. Patent No. 5,860,092 combines an adder with a pre-decoder circuit to provide an input to a word-line driver. Figures 2

shows this prior art method. One disadvantage with these two methods is that carry propagation for larger addresses can adversely affect cache access time.

In another prior art method, Cortadella et al (in "Evaluation of A+B=K Conditions Without Carry Propagation," IEEE Transactions on Computers, vol. 41, pp. 1484-1488, Nov., 1992) show that an equality test does not require carry propagation. One representation of a sum A+B, which is suitable for use in a carry nonpropagative equality test, is known as half-adder or carry-sum form. The carry-sum representation uses a carry bit, C_i, and a sum bit, S_i, to represent a binary digit of a number in the ith digit position. In carry-sum form each number may have multiple valid representations. In a system of numbers, where each number is assigned multiple binary representations, the numbers are said to be in redundant form.

Current processors make use of pipelining to reduce cycle times and exploit parallelism within instruction streams. In order to make pipelining efficient, results from digital arithmetic circuitry are bypassed back to circuit inputs as operands for the next operation in a pipeline. This technique is preferred over one of waiting until results are written back to a register file, and it provides for higher utilization of a pipeline's parallelism. Since quickly loading operands from memory is critical to the performance of a processor, it may be desirable to bypass results of address computations to a load/store unit in order to reduce any delays associated with the load.

When bypassed addresses are used to access cache it is desirable to have a cache that can decode addresses in redundant form. When address calculations have time to complete, the addresses are already converted to a unsigned binary number and so a traditional decoder is desirable. Often, a design decision must be made to store all addresses to one or the other form because two decoders require too much in area resorces.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings.

Figure 1 shows a prior art adder/decoder.

Figure 2 shows another prior art adder/decoder.

Figure 3 shows a carry-save adder circuit.

Figure 4a shows a ROM implementation of a 3:2 compressor or counter based on the truth table for addition in a carry-sum redundant form.

Figure 4b shows a half adder circuit, which can be used as a building block to construct a full adder circuit.

Figure 4c shows a 3:2 compressor or counter that can be used to form the basic building block of a carry-save adder.

Figure 5 shows a cache wordline decoder for decoding addresses in a carry-sum redundant form.

Figure 6 shows one embodiment of a pre-decoder component circuit that accepts addresses in a carry-sum redundant form.

Figure 7 shows another embodiment of a pre-decoder component circuit that accepts addresses in a negated carry-sum redundant form.

Figure 8 shows one embodiment of a decoder component circuit that combines two-bit subsequences into three-bit subsequences.

Figure 9 details one embodiment of a cache wordline decoder for decoding four-digit addresses in a carry-sum redundant form.

Figure 10a shows one embodiment of a circuit for selectively replacing one redundant representation bit with a constant bit for addresses in a redundant form.

Figure 10b shows another embodiment of a circuit for selectively replacing one redundant representation bit with a constant bit for addresses in a negated redundant form.

Figure 11 shows another embodiment of a pre-decoder component circuit that accepts addresses in a carry-sum redundant form and provides selective replacement of one redundant representation bit vector with a constant bit vector.

Figure 12 shows one embodiment of a cache wordline decoder for carry-sum redundant load addresses and unsigned binary store addresses that provides selective replacement of one redundant representation bit vector with a constant bit vector.

Figure 13a shows one embodiment of circuit that accepts addresses in a sign-digit redundant form and provides addresses in a negated carry-sum redundant form.

Figure 13b shows of circuit that accepts addresses in a sign-digit redundant form, provides selective replacement of one redundant representation bit vector with a constant bit vector and provides addresses in a negated carry-sum redundant form.

Figure 14 shows another embodiment of a pre-decoder component circuit that accepts addresses in a sign-digit redundant form and provides selective replacement of one redundant representation bit vector with a constant bit vector.

Figure 15 shows another embodiment of a cache wordline decoder for sign-digit redundant load addresses and unsigned binary store addresses that provides selective replacement of one redundant representation bit vector with a constant bit vector.

Figure 16 shows one embodiment of a digital computing system comprising a cache wordline decoder for redundant load addresses and unsigned binary store addresses that provides selective replacement of one redundant representation bit vector with a constant bit vector.

Figure 17 shows one embodiment of a method of cache wordline decoding for redundant addresses or unsigned binary addresses using selective replacement of one redundant representation bit vector with a constant bit vector.

DETAILED DESCRIPTION

These and other embodiments of the present invention may be realized in accordance with the following teachings and it should be evident that various modifications and changes may be made in the following teachings without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense and the invention measured only in terms of the claims.

In one embodiment, a cache wordline decoder, herein described, provides pre-decode circuitry to identify subsequences from redundant addresses and can be configured to also identify subsequences from unsigned binary addresses for decoding into identified wordline sequences. The wordline sequences are used to access data stored in cache memory at corresponding storage locations. Since data in memory requested by a load operation is desired more urgently than result data needs to be written back into memory, a disclosed embodiment of a cache wordline decoder provides a way to process load requests without waiting for load address calculations to be completed. But since store address calculations typically have time to finish, this embodiment of a cache wordline decoder provides a way to process store requests without requiring a second wordline decoder for unsigned binary addresses.

One method for quickly calculating load addresses is to use a carry nonpropagative arithmetic circuit such as a carry-save adder to sum addressing

components, possibly including a base address and an index or a displacement. Results from a carry-save adder can be bypassed to a load-store unit in redundant form, without waiting for carry propagation to complete.

A carry save adder is shown in Figure 3. The carry save adder has a structure very similar to that of a traditional adder except for eliminating the need to propagate carry signals generated in a first stage, 301, along the length of the result in a second stage, 302. When adding two of these numbers together, circuits, 303, which are similar to traditional half adders and 3:2 compressors can be used. Figure 4a shows a truth table for the 3:2 compressor, which could be implemented in a read-only memory (ROM). Figure 4b shows the traditional half adder circuit, and Figure 4c shows a 3:2 compressor circuit that can be used to form the basic building block, 303, of a carry save adder.

In order to access cache using such an address, a cache wordline decoder for decoding addresses in a carry-sum redundant form is required. The type of cache wordline decoder required is depicted in Figure 5. It accepts addresses in which the binary digits comprise carry bits, C_i, and sum bits, S_i, produced by a carry-save adder. In order to identify a corresponding wordline, $Wordline^i$, in cache memory, adjacent digits can first be pre-decoded by pre-decoder 501 to identify possible subsequences that could result from completion of carry propagation. According to the identified possible subsequences, subsequence indicators in subsequence indicator sets 502, 503, 504, and 505, 506 are

activated. These subsequence indicators are combined in decoder 507 to identify a unique wordline sequence. According to the wordline sequence identified, one of a set of wordline indicators 508 is activated to access a corresponding location in cache.

Identification of possible subsequences from carry-sum redundant digits can be accomplished using a circuit like the one shown in Figure 6. This embodiment of a pre-decoder component circuit 608 comprises pre-decoder component circuit 604 and pre-decoder component circuit 602. Pre-decoder component circuit 604 accepts, sum bits, S_i and S_{i-1}, and carry bits, C_{i-1} and C_{i-2}, of an address in carry-sum redundant form and identifies possible two-bit subsequences that could result at positions, i and i-1 when the carry-sum address is converted into two's complement form. The identified possible subsequences are indicated by activating at least one of the four possible subsequence indicator signals, R_i^{11}, R_i^{01}, $R_i^{10}$and R_i^{00}. Likewise, sum bits, S_{i-1} and S_{i-2}, and carry bits, C_{i-2} and C_{i-3}, can be used by pre-decoder component circuit 602 to identify possible two-bit subsequences that could result at positions, i-1 and i-2 when the address is converted to two's complement. The possible subsequences are indicated by activating at least one of the four possible subsequence indicator signals, R_{i-1}^{11} ,R_{i-1}^{01}, R_{i-1}^{10}, R_{i-1}^{00}.

As shown in Figure 6, the afore mentioned possible subsequence indicator signals (as shown in pre-decoder component circuit 604) for a subsequence

with most significant bit at position, i, in a wordline sequence are activated according to the following logic equations or their equivalents:

$$R_i^{11} = (S_{i-1} \text{ AND } C_{i-2}) \text{ XOR } (S_i \text{ XOR } C_{i-1}),$$

$$R_i^{01} = (S_{i-1} \text{ AND } C_{i-2}) \text{ XNOR } (S_i \text{ XOR } C_{i-1}),$$

$$R_i^{10} = (S_{i-1} \text{ OR } C_{i-2}) \text{ XOR } (S_i \text{ XOR } C_{i-1}),$$

$$R_i^{00}. = (S_{i-1} \text{ OR } C_{i-2}) \text{ XNOR } (S_i \text{ XOR } C_{i-1}).$$

Another embodiment of a circuit for identification of possible subsequences from negated carry-sum redundant digits is shown in Figure 7. This embodiment of a pre-decoder component circuit 708 comprises pre-decoder component circuit 704 and pre-decoder component circuit 702. Pre-decoder component circuit 704 accepts, negated sum bits, not S_i and not S_{i-1}, and negated carry bits, not C_{i-1} and not C_{i-2}, of an address in carry-sum redundant form and identifies possible two-bit subsequences that could result at positions, i and i-1 when the carry-sum address is converted into unsigned binary form. The identified possible subsequences are indicated by activating at least one of the four signals, R_i^{11}, R_i^{01}, $R_i^{10}$and R_i^{00}. Likewise, negated sum bits, not S_{i-1} and not S_{i-2}, and negated carry bits, not C_{i-2} and not C_{i-3}, can be used by pre-decoder component circuit 702 to identify possible two-bit subsequences that could result at positions, i-1 and i-2 when the address is converted to unsigned binary. The possible subsequences are indicated by activating at least one of the four signals, R_{i-1}^{11} ,R_{i-1}^{01}, R_{i-1}^{10}, R_{i-1}^{00}.

As shown in Figure 7, the afore mentioned possible subsequence indicator signals (as shown in pre-decoder component circuit 704) for a subsequence with most significant bit at position, i, in a wordline sequence are activated according to the following logic equations or their equivalents:

$$R_i^{11} = (\text{ NOT } S_{i-1} \text{ NOR NOT } C_{i-2}) \text{ XOR } (\text{NOT } S_i \text{ XOR NOT } C_{i-1}),$$

$$R_i^{01} = (\text{NOT } S_{i-1} \text{ NOR NOT } C_{i-2}) \text{ XNOR } (\text{NOT } S_i \text{ XOR NOT } C_{i-1}),$$

$$R_i^{10} = (\text{NOT } S_{i-1} \text{ NAND NOT } C_{i-2}) \text{ XOR } (\text{NOT } S_i \text{ XOR NOT } C_{i-1}),$$

$$R_i^{00}. = (\text{NOT } S_{i-1} \text{ NAND NOT } C_{i-2}) \text{ XNOR } (\text{NOT } S_i \text{ XOR NOT } C_{i-1}).$$

The possible three-bit subsequences ending at position, i, can be identified by combining possible two-bit sequences ending at position, i, with the possible two-bit subsequences ending at position, i-1. Figure 8 shows one embodiment of a decoder component circuit that combines two-bit subsequences into three-bit subsequences in this manner. It should be noted, of course, that one skilled in the art could modify the pre-decoders illustrated in Figures 6 and 7 to directly identify possible three-bit subsequences, or to identify possible four-bit subsequences, or to identify possible subsequences of any other size.

As shown in Figure 8, a 3-bit possible subsequence indicator for a subsequence with most significant bit at position, i, in a wordline sequence is activated according to the following logic equations or their equivalents:

$$R_i^{111} = R_i^{11} \text{ AND } R_{i-1}{}^{11},$$

$$R_i^{110} = R_i^{11} \text{ AND } R_{i-1}{}^{10},$$

$$R_i^{101} = R_i^{10} \text{ AND } R_{i-1}{}^{01},$$

$R_i^{100} = R_i^{10}$ AND R_{i-1}^{00},

$R_i^{011} = R_i^{01}$ AND R_{i-1}^{11},

$R_i^{010} = R_i^{01}$ AND R_{i-1}^{10},

$R_i^{001} = R_i^{00}$ AND R_{i-1}^{01}, and

$R_i^{000} = R_i^{00}$ AND R_{i-1}^{00}.

In a like manner, longer subsequences could be identified by ANDing together additional subsequences.

One embodiment of a cache wordline decoder for decoding four-digit binary addresses in a carry-sum redundant form is illustrated in Figure 9. Through combining the possible two-bit subsequences ending at position, i, identified by pre-decoder component circuit 908; position i-1, identified by pre-decoder component circuit 904; and position i-2, identified by pre-decoder component circuit 902; position with the one-bit possibilities for the least significant position, identified by pre-decoder component circuit 901 the unique four-bit wordline corresponding to the carry-sum redundant address can be identified without requiring carry propagation.

A unique wordline indicator for a 4-bit wordline sequence is activated by decoder 916 according to the following logic equations or their equivalents:

$Word^{1111} = R_3^{11}$ AND R_2^{11} AND R_1^{11} AND R_0^{1X},

$Word^{1110} = R_3^{11}$ AND R_2^{11} AND R_1^{10} AND R_0^{0X},

$Word^{1101} = R_3^{11}$ AND R_2^{10} AND R_1^{01} AND R_0^{1X},

$Word^{1100} = R_3^{11}$ AND R_2^{10} AND R_1^{00} AND R_0^{0X},

$$Word^{1011} = R_3^{10} \text{ AND } R_2^{01} \text{ AND } R_1^{11} \text{ AND } R_0^{1X},$$

$$Word^{1010} = R_3^{10} \text{ AND } R_2^{01} \text{ AND } R_1^{10} \text{ AND } R_0^{0X},$$

$$Word^{1001} = R_3^{10} \text{ AND } R_2^{00} \text{ AND } R_1^{01} \text{ AND } R_0^{1X},$$

$$Word^{1000} = R_3^{10} \text{ AND } R_2^{00} \text{ AND } R_1^{00} \text{ AND } R_0^{0X},$$

$$Word^{0111} = R_3^{01} \text{ AND } R_2^{11} \text{ AND } R_1^{11} \text{ AND } R_0^{1X},$$

$$Word^{0110} = R_3^{01} \text{ AND } R_2^{11} \text{ AND } R_1^{10} \text{ AND } R_0^{0X},$$

$$Word^{0101} = R_3^{01} \text{ AND } R_2^{10} \text{ AND } R_1^{01} \text{ AND } R_0^{1X},$$

$$Word^{0100} = R_3^{01} \text{ AND } R_2^{10} \text{ AND } R_1^{00} \text{ AND } R_0^{0X},$$

$$Word^{0011} = R_3^{00} \text{ AND } R_2^{01} \text{ AND } R_1^{11} \text{ AND } R_0^{1X},$$

$$Word^{0010} = R_3^{00} \text{ AND } R_2^{01} \text{ AND } R_1^{10} \text{ AND } R_0^{0X},$$

$$Word^{0001} = R_3^{00} \text{ AND } R_2^{00} \text{ AND } R_1^{01} \text{ AND } R_0^{1X}, \text{ and}$$

$$Word^{0000} = R_3^{00} \text{ AND } R_2^{00} \text{ AND } R_1^{00} \text{ AND } R_0^{0X}.$$

In Figure 10a, one embodiment of a circuit for selectively replacing 1010 one bit of a bit vector of an address in redundant form with a constant bit is illustrated. When redundant enable, REN, is asserted, a signal C_i will propagate through the NAND structure 1011 and the inverter 1013 to produce C_i at the output. When REN is negated, a constant low logic level will be produced.

In Figure 10b, another embodiment of a circuit for selectively replacing one bit of an address in negated redundant form with a constant bit is illustrated. When low active redundant enable, REN bar, is asserted, an input signal, not

C_i, will propagate through the NOR structure 1020 to produce C_i at the output. When REN bar is high, a constant low logic level will be produced.

The circuit of Figure 10a can be used in a pre-decode component circuit to replace the carry bit vector with a constant bit vector. Figure 11 shows an embodiment of a pre-decoder component circuit that accepts an address in a carry-sum redundant form and provides selective replacement of the carry bit vector with a constant bit vector. By selecting the correct constant, an address in unsigned binary form can be accepted as the sum bit vector and the resulting cache wordline decoder can be used for either redundant addresses or unsigned binary addresses. For example, if redundant enable signal, REN, is asserted on select input 1101, then the carry signal C_{i-3} on bit vector input 1102 propagates through the AND structure 1110 undergoing two inversions to input 1104 of the pre-decode component circuit 1112 where it is combined with S_{i-2} on bit vector input 1105, S_{i-1} on bit vector input 1107, and similarly processed C_{i-2} at the bit vector replacement output 1606. On the other hand, if redundant enable signal, REN, is low on select input 1101, then the carry signal C_{i-3} on bit vector input 1102 does not propagate through the AND structure 1110, but rather the low value of REN propagates a zero to input 1104 of the pre-decode component circuit 1112 where it is combined with S_{i-2} on bit vector input 1105, S_{i-1} on bit vector input 1107, and a similarly produced zero at the bit vector replacement output 1606.

One embodiment of a cache wordline decoder for carry-sum redundant load addresses represented by a sum bit vector, S, and a carry bit vector, C, or unsigned binary store addresses represented by the linear bit vector, A, is depicted in Figure 12. Pre-decode circuitry 1201 provides selective replacement of the carry bit vector with a constant bit vector, responsive to negation of a redundant enable control signal, REN. The decoding is then allowed to proceed as usual. In order to identify a corresponding wordline, Wordline^i, in cache memory, adjacent digits can first be pre-decoded by pre-decoder 1201 to identify possible subsequences that could result from completion of carry propagation. According to the identified possible subsequences, subsequence indicators in subsequence indicator sets 1202, 1203, 1204, and 1205, 1206 are activated. These subsequence indicators are combined in decoder 1207 to identify a unique wordline sequence. According to the wordline sequence identified, one of a set of wordline indicators 1208 is activated to access a corresponding location in cache.

Another redundant representation used to quickly calculate load addresses without carry propagation is the sign-digit redundant form. In the sign-digit redundant form, each digit is represented by sign bit, X_{si}, and a magnitude bit, X_{mi}. Figure 13a shows one embodiment of circuit that accepts addresses in a sign-digit redundant form and produces addresses in a negated carry-sum redundant form. A least significant digit 1311 is produced by negating X_{m0} to produce a negated sum bit, S_0 bar, while X_{s0} and X_{m0} are combined through an

AND gate to produce C_0 bar. Other digits, including a most significant digit 1319 are produced by propagating each X_{mi} to produce each negated sum bit, S_i bar, while NOT X_{si} and X_{mi} are combined through a NAND gate to produce C_i bar.

Figure 13b shows another embodiment of a bit vector selection or bit vector replacement circuit including, a least significant digit replacement circuit 1321 and a most significant replacement circuit 1329, that accepts addresses in a sign-digit redundant form and provides selective replacement of the sign bit vector with a constant bit vector producing addresses in a negated carry-sum redundant form. Combining this circuit with the pre-decode component circuit depicted in Figure 7 produces the embodiment illustrated in Figure 14.

In Figure 14, a pre-decoder component circuit that accepts addresses in a sign-digit redundant form provides selective replacement of the sign bit vector with a constant bit vector. By selecting the correct constant, an address in unsigned binary form can be accepted as the magnitude bit vector and the resulting cache wordline decoder can be used for either redundant addresses or unsigned binary addresses.

One embodiment of a cache wordline decoder for sign-digit redundant load addresses represented by a sign bit vector, X_s, and a magnitude bit vector, X_m, or unsigned binary store addresses represented by the linear bit vector, A, is depicted in Figure 15. Pre-decode circuitry 1501 provides selective replacement of the sign bit vector with a constant bit vector, responsive to negation of a redundant enable control signal, REN. The decoding is again

allowed to proceed as usual. In order to identify a corresponding wordline, Wordline^{i}, in cache memory, adjacent digits can first be pre-decoded by pre-decoder 1501 to identify possible subsequences that could result from completion of carry propagation. According to the identified possible subsequences, subsequence indicators in subsequence indicator sets 1502, 1503, 1504, and 1505, 1506 are activated. These subsequence indicators are combined in decoder 1507 to identify a unique wordline sequence. According to the wordline sequence identified, one of a set of wordline indicators 1508 is activated to access a corresponding location in cache.

One embodiment of a digital computing system is shown in Figure 16, which comprises a cache wordline decoder,1611, for receiving redundant load addresses and unsigned binary store addresses. In one embodiment, cache 1611, is the fastest cache in a hierarchical plurality of caches including slower external caches and 1611 is resident on the same die as processor, 1610. In another embodiment, cache 1611 and possibly other internal caches reside on the same die, but there are no external caches.

Instruction decoder, 1601, receives instructions that may include additions, loads, stores, etc. For example, an first instruction to add a base address in a first register to an index in a second register, writing the result in a third register may be received and decoded. Then a second instruction to load data from the address in the third register may be received and decoded. The first instruction may produce a result by providing operands from a register file, 1605, to a

redundant adder, 1603. In order to complete the second instruction quickly, the result produced by redundant adder, 1603, may be bypassed to a cache, 1611, by the bypassing control 1607. Control unit, 1602, asserts redundant enable (REN) to direct pre-decoder, 1609, to handle the address in redundant form.

On the other hand, a third instruction to store a new result back to the address location found in the third register may be received. In this case the result produced by redundant adder, 1603, in the first instruction may have already been converted to unsigned binary form by redundant conversion unit, 1604, and written into register file, 1605. Therefore the contents of the third register are sent to the cache, 1611, and control unit, 1602, negates REN to direct the pre-decoder, 1609, to provide selective replacement of one redundant representation bit vector with a constant bit vector, thereby correctly decoding the unsigned binary address received.

In Figure 17 one embodiment of a method of wordline decoding for redundant addresses or unsigned binary addresses in a cache is illustrated. After receiving an address comprising a first bit vector and a second bit vector, 1701, at the cache, a check is performed to determine if redundant addressing is enabled, 1702. If it is enabled, subsequences of the first bit vector are combined, 1704, with subsequences of the second bit vector to identify possible result subsequences. The result subsequences are then combined, 1705, to identify the unique wordline represented by the redundant address, and data stored at the identified wordline is accessed, 1706.

On the other hand, if redundant addressing is not enabled, 1702, then a selective replacement, 1703, of one redundant representation bit vector with a constant bit vector is performed. Subsequences of the original bit vector and the replaced bit vector are then combined, 1704, as before to identify possible result subsequences. Finally, these result subsequences are then combined, 1705, to identify the unique wordline represented by the redundant address, and data stored at the identified wordline is accessed, 1706.

The above description is intended to illustrate preferred embodiments of the present invention. From the discussion above it should also be apparent that the invention can be modified in arrangement and detail by those skilled in the art without departing from the principles of the present invention within the scope of the accompanying claims.

CLAIMS

What is claimed is:

1. An apparatus for accessing data in a memory, the apparatus comprising:

a bit vector replacement circuit to receive a first bit vector and a control signal and to substitute a constant bit vector for the first bit vector, in response to the control signal being in a first state, to produce a second bit vector;

a pre-decoder coupled with the bit vector replacement circuit to receive a plurality of bit vectors including the second bit vector, to combine subsequences from the plurality of bit vectors to identify possible wordline subsequences corresponding to the plurality of bit vectors, and to activate a subsequence indicator for an identified possible wordline subsequence; and

a wordline decoder coupled with the pre-decoder to combine activated subsequence indicators to identify a unique wordline corresponding to the plurality of bit vectors.

2. The apparatus of Claim 1, wherein the plurality of bit vectors correspond to an address represented in carry-sum redundant form.

3. The apparatus of Claim 1, wherein the plurality of bit vectors comprise:

a carry bit vector including a carry bit corresponding to a binary digit of the address; and

a sum bit vector including a sum bit corresponding to a binary digit of the address.

4. The apparatus of Claim 3, wherein the first bit vector is the carry bit vector.

5. The apparatus of Claim 4, wherein the second bit vector produced by the bit vector replacement circuit in response to the control signal being in a second state corresponds to the carry bit vector.

6. The apparatus of Claim 1, wherein the plurality of bit vectors correspond to an address represented in sign-digit redundant form.

7. The apparatus of Claim 6, wherein the plurality of bit vectors comprise:

a sign bit vector including a sign bit corresponding to a binary digit of the address; and

a magnitude bit vector including a magnitude bit corresponding to a binary digit of the address.

8. The apparatus of Claim 7, wherein the first bit vector is the sign bit vector.

9. The apparatus of Claim 8, wherein the second bit vector produced by the bit vector replacement circuit in response to the control signal being in a second state corresponds to the sign bit vector.

10. The apparatus of Claim 1, wherein the vector replacement circuit substitutes a constant bit vector corresponding to a zero vector for the first bit vector.

11. The apparatus of Claim 1, wherein the pre-decoder is a carry nonpropagative circuit.

12. The apparatus of Claim 11, wherein the pre-decoder identifies possible two-bit wordline subsequences.

13. The apparatus of Claim 11, wherein the pre-decoder activates a subsequence indicator for an identified possible two-bit subsequence.

14. The apparatus of Claim 1, wherein one of the plurality of bit vectors corresponds to an address represented in unsigned binary form.

15. The apparatus of Claim 14, wherein said one of the plurality of bit vectors corresponds to a store address.

16. The apparatus of Claim 1, further comprising:

a cache coupled with the wordline decoder to store a copy of a datum stored in the memory, the copy being stored at a wordline in the cache corresponding to an address in the memory.

17. The apparatus of Claim 16, further comprising:

a processor coupled with the pre-decoder to produce the plurality of bit vectors.

18. The apparatus of Claim 17, wherein the processor produces one or more of the plurality of bit vectors by adding together addressing components including a base address and an index or a displacement.

19. A digital computing system comprising:

a die;

a bit vector selection circuit on the die to receive a first bit vector and a control signal, and to select a constant bit vector or the first bit vector responsive to the control signal, and to output the selected bit vector as a second bit vector;

a decoder circuit on the die coupled to the bit vector selection circuit to receive a plurality of bit vectors including the second bit vector and to combine a subsequence from each of the plurality of bit vectors to identify a

wordline corresponding to the plurality of bit vectors;

an internal cache on the die, the internal cache coupled with the decoder circuit to store a first datum at the wordline corresponding to the plurality of bit vectors;

a processor on the die coupled with the decoder circuit to produce the plurality of bit vectors; and

an external cache, not on the die, to store a second datum, the external cache coupled with the die and with the internal cache, to transmit the second datum to the internal cache to be stored on the die.

20. The digital computing system of Claim 19, wherein the plurality of bit vectors correspond to an address represented in carry-sum redundant form and the plurality of bit vectors comprise:

a carry bit vector including a carry bit corresponding to a binary digit of the address; and

a sum bit vector including a sum bit corresponding to a binary digit of the address.

21. The digital computing system of Claim 20, wherein the first bit vector is the carry bit vector.

22. The digital computing system of Claim 19, wherein one of the plurality of bit vectors corresponds to an address represented in unsigned binary form.

23. The apparatus of Claim 22, wherein said one of the plurality of bit vectors corresponds to a store address.

24. A cache memory system comprising:

a plurality of lines for storing copies of memory storage locations having corresponding addresses;

means for decoding an address to access a line of the cache memory system responsive to an access request that includes an address represented in a redundant form; and

means for decoding an address to access a line of the cache memory system responsive to an access request that includes an address represented in unsigned binary form.

25. A method of accessing data in a first storage, the method comprising:

copying a plurality of storage locations from a second storage into a plurality of lines of the first storage by asserting corresponding line signals;

receiving an access request including a first bit vector, a second bit vector and a control signal;

setting the second bit vector equal to a constant bit vector if the control

signal is in a first state;

identifying a line corresponding to the combined first bit vector and second bit vector:

asserting the identified line signal; and

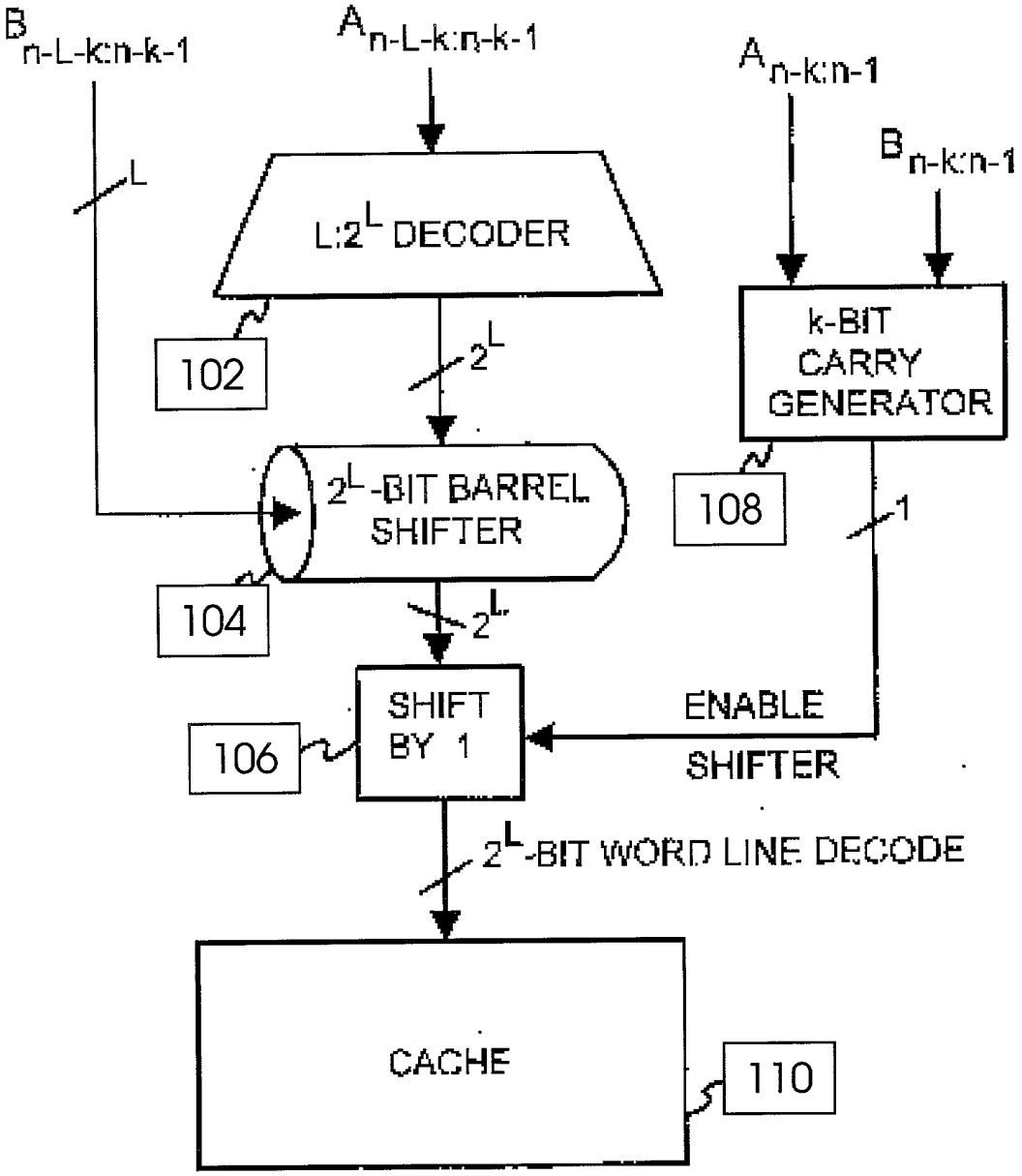
accessing the line of the first storage corresponding to the asserted line signal.

ABSTRACT OF THE DISCLOSURE

In one embodiment, a wordline decoder provides access to cache memory locations when addresses are bypassed directly from arithmetic circuitry in redundant form. The wordline decoder is also designed to provide access to cache memory locations when addresses are received from registers in an unsigned binary form. The combined functionality is provided in a pre-decode circuit by selectively replacing one of a plurality of redundant bit vectors with a constant bit vector when redundant addressing is not enabled.

PRIOR ART

FIG. 1



PRIOR ART

FIG. 2

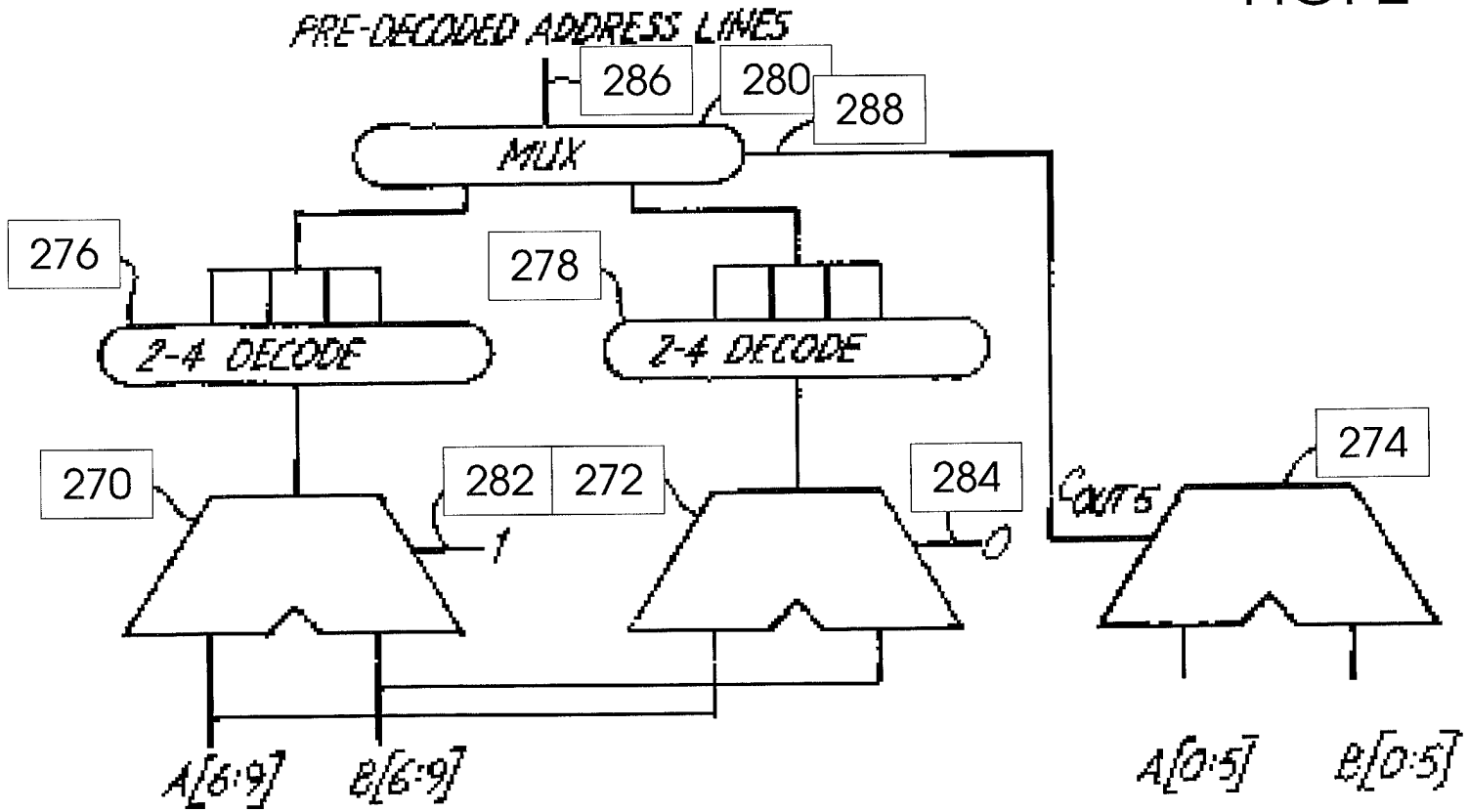


FIG. 3

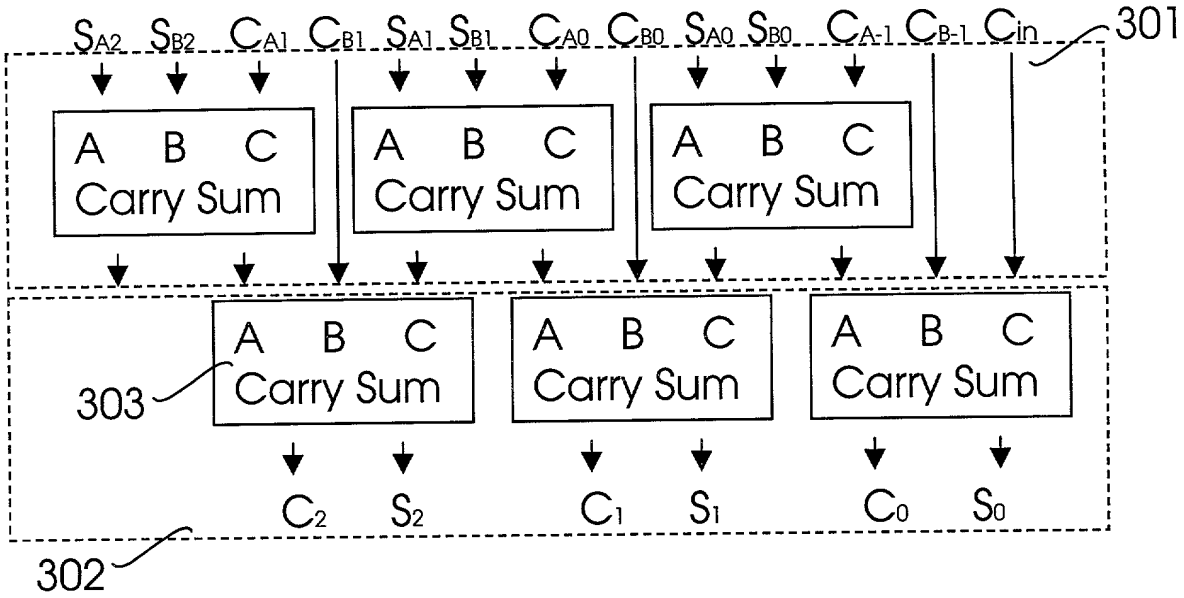


FIG. 4a

3:2 Compressor

ROM Address	ROM Data	
0 0 0	0	0
0 0 1	0	1
0 1 0	0	1
0 1 1	1	0
1 0 0	0	1
1 0 1	1	0
1 1 0	1	0
1 1 1	1	1
A B C	**Carry Sum**	

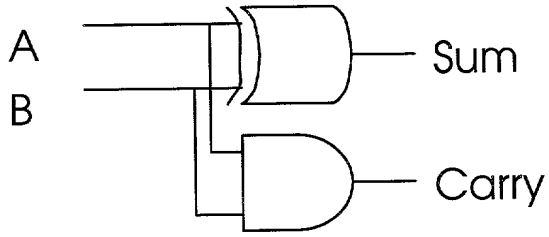


FIG. 4b

FIG. 4c

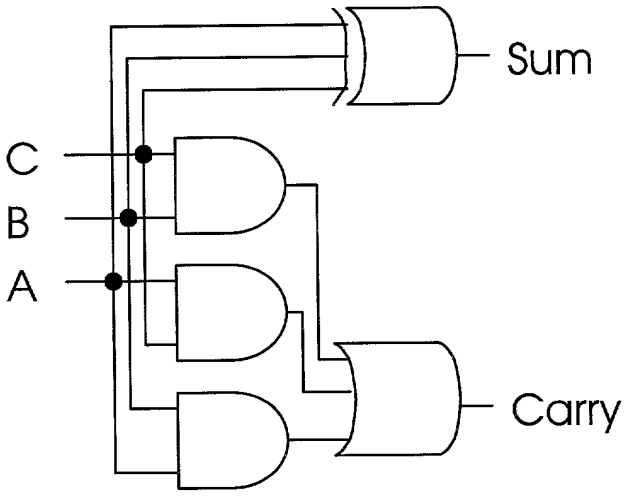


FIG. 5

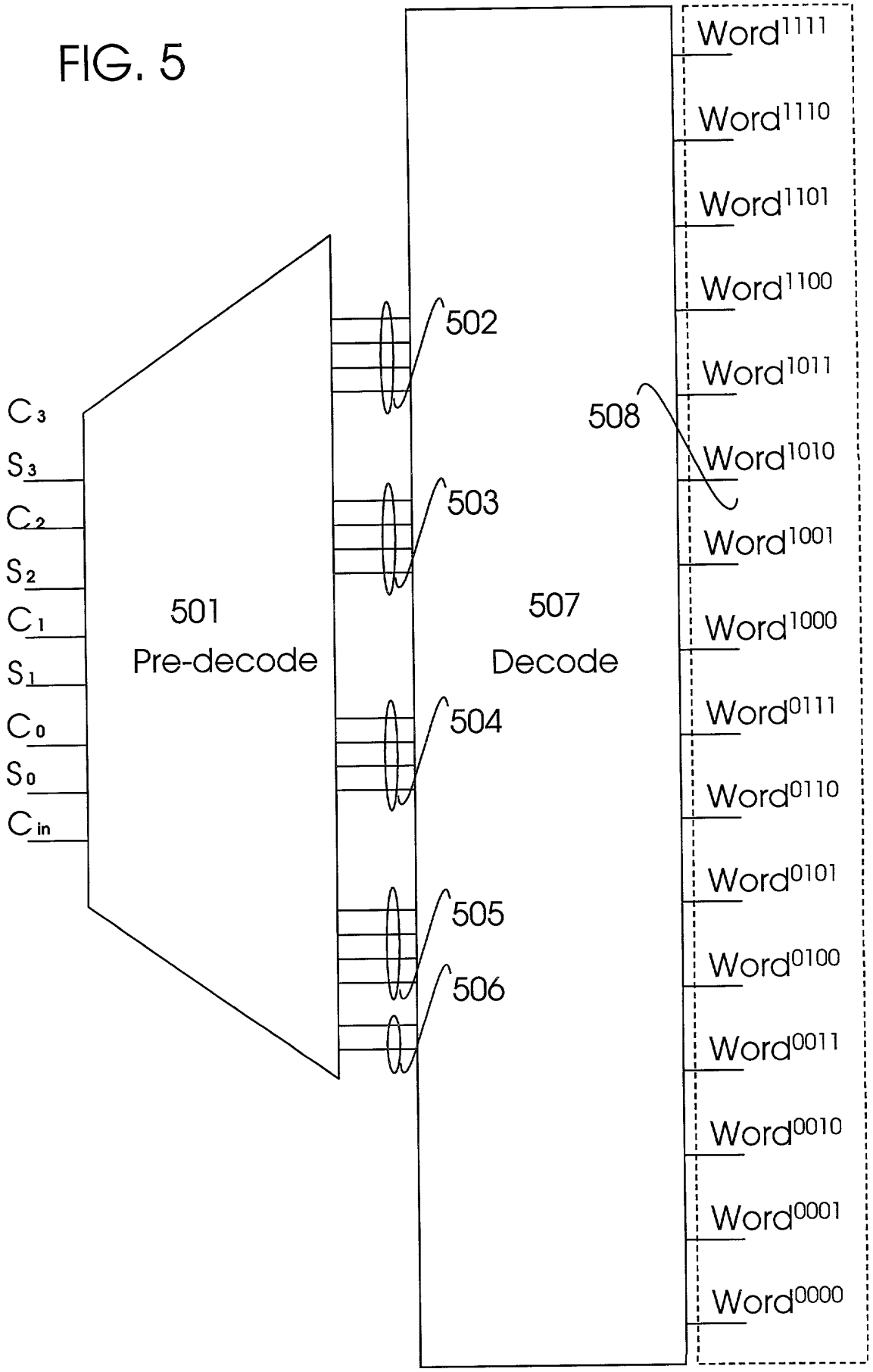

C_3
S_3
C_2
S_2
C_1
S_1
C_0
S_0
C_{in}
501
Pre-decode
502
503
504
505
506
507
Decode
508
$Word^{1111}$
$Word^{1110}$
$Word^{1101}$
$Word^{1100}$
$Word^{1011}$
$Word^{1010}$
$Word^{1001}$
$Word^{1000}$
$Word^{0111}$
$Word^{0110}$
$Word^{0101}$
$Word^{0100}$
$Word^{0011}$
$Word^{0010}$
$Word^{0001}$
$Word^{0000}$

FIG. 6

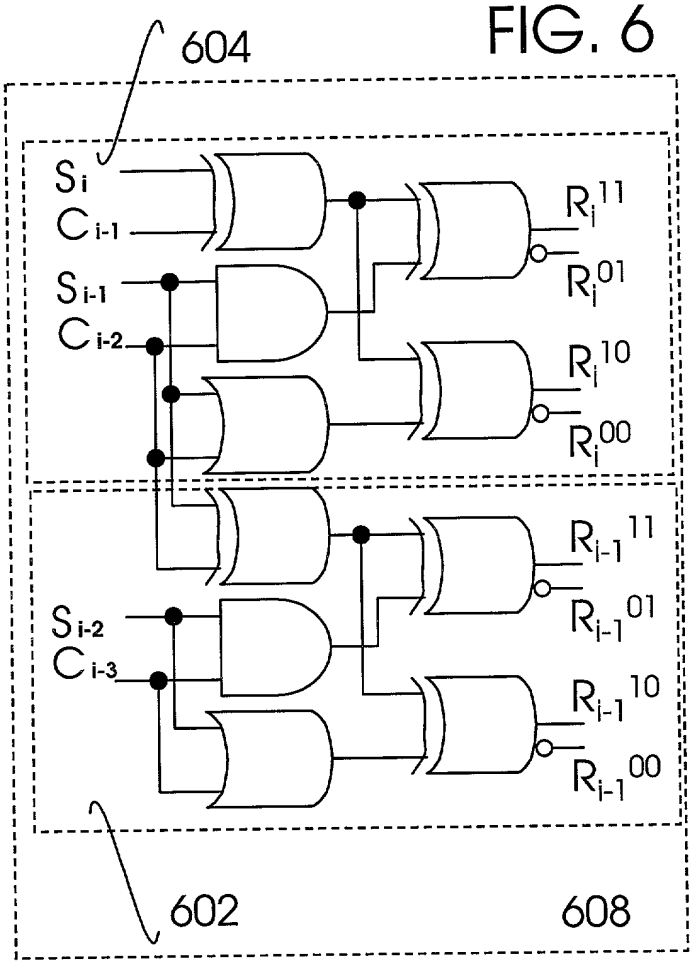

604
S_i
C_{i-1}
S_{i-1}
C_{i-2}
S_{i-2}
C_{i-3}
R_i^{11}
R_i^{01}
R_i^{10}
R_i^{00}
R_{i-1}^{11}
R_{i-1}^{01}
R_{i-1}^{10}
R_{i-1}^{00}
602
608

FIG. 7

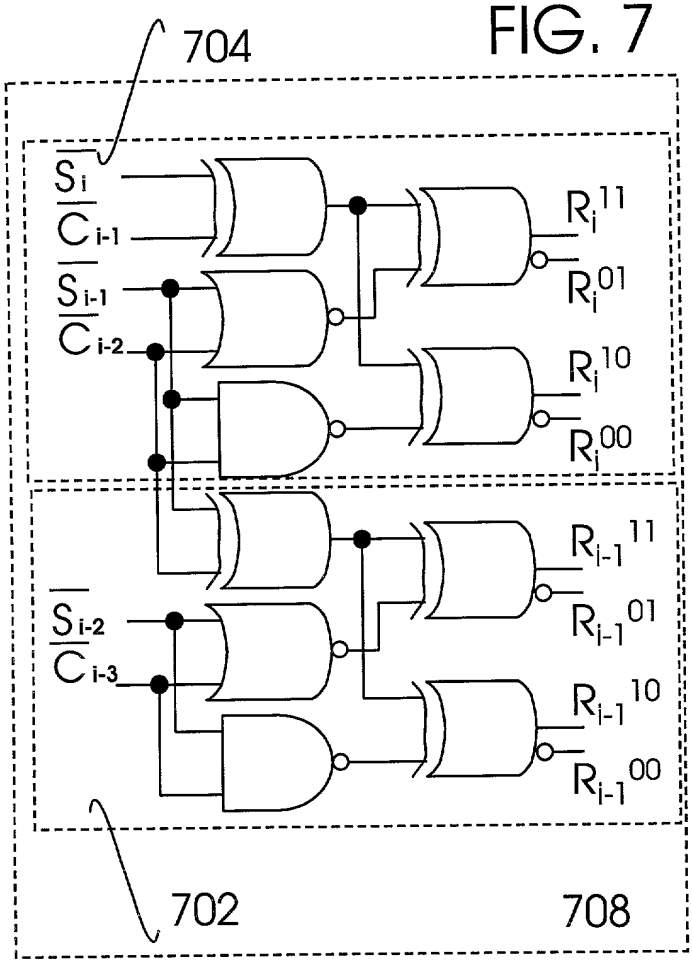

704
$\overline{S_i}$
$\overline{C_{i-1}}$
$\overline{S_{i-1}}$
$\overline{C_{i-2}}$
R_i^{11}
R_i^{01}
R_i^{10}
R_i^{00}
$\overline{S_{i-2}}$
$\overline{C_{i-3}}$
R_{i-1}^{11}
R_{i-1}^{01}
R_{i-1}^{10}
R_{i-1}^{00}
702
708

FIG. 8

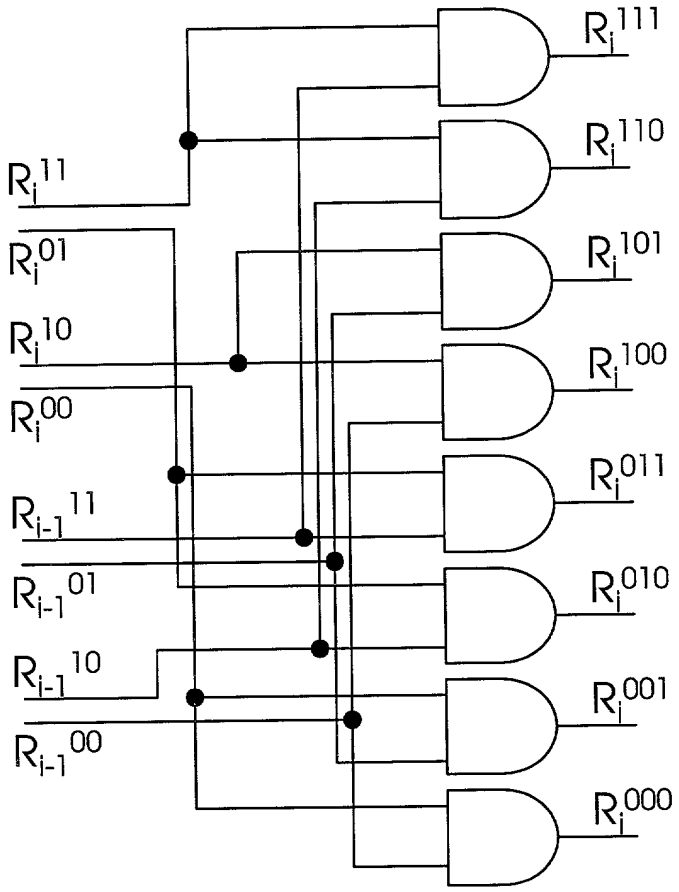
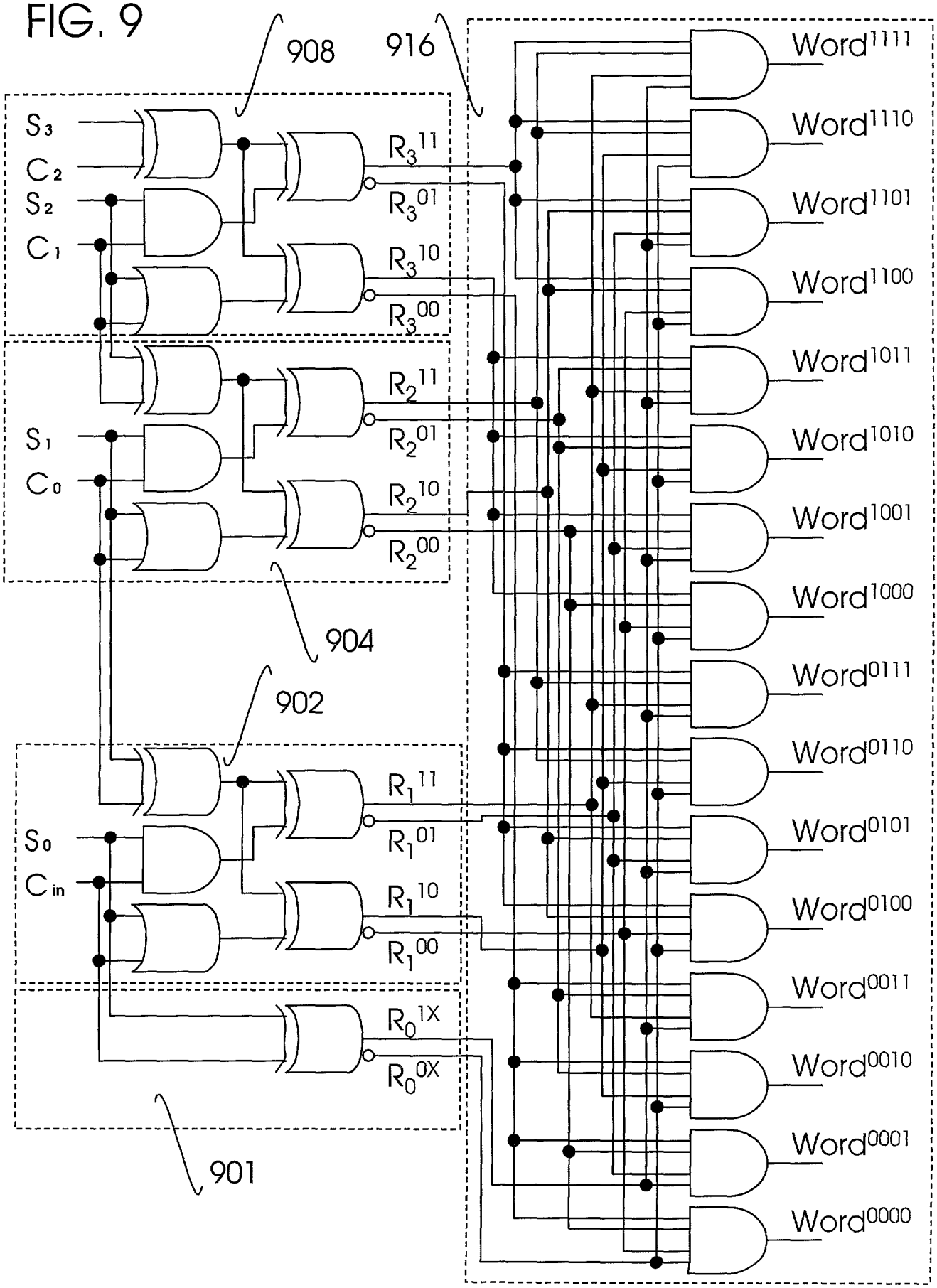

R_i^{111}
R_i^{110}
R_i^{11}
R_i^{101}
R_i^{01}
R_i^{100}
R_i^{10}
R_i^{011}
R_i^{00}
R_{i-1}^{11}
R_i^{010}
R_{i-1}^{01}
R_i^{001}
R_{i-1}^{10}
R_i^{000}
R_{i-1}^{00}

FIG. 9


908
916
S3
C2
S2
C1
R3^11
R3^01
R3^10
R3^00
S1
C0
R2^11
R2^01
R2^10
R2^00
904
902
S0
Cin
R1^11
R1^01
R1^10
R1^00
R0^1X
R0^0X
901
Word^1111
Word^1110
Word^1101
Word^1100
Word^1011
Word^1010
Word^1001
Word^1000
Word^0111
Word^0110
Word^0101
Word^0100
Word^0011
Word^0010
Word^0001
Word^0000

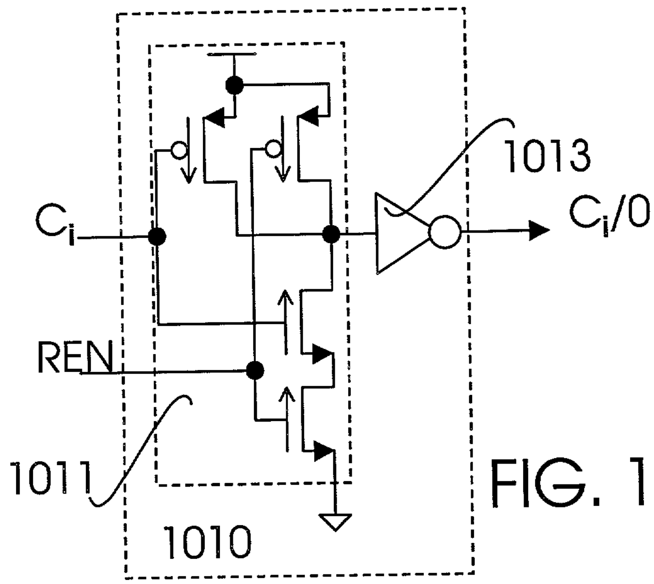


FIG. 10a

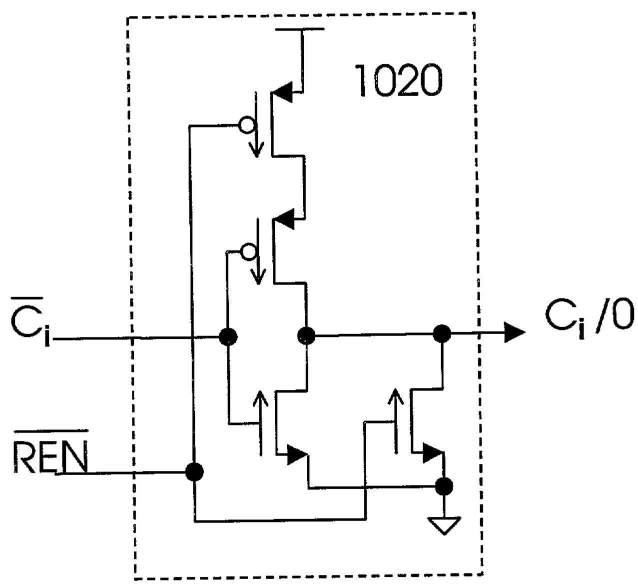


FIG. 10b

FIG. 11

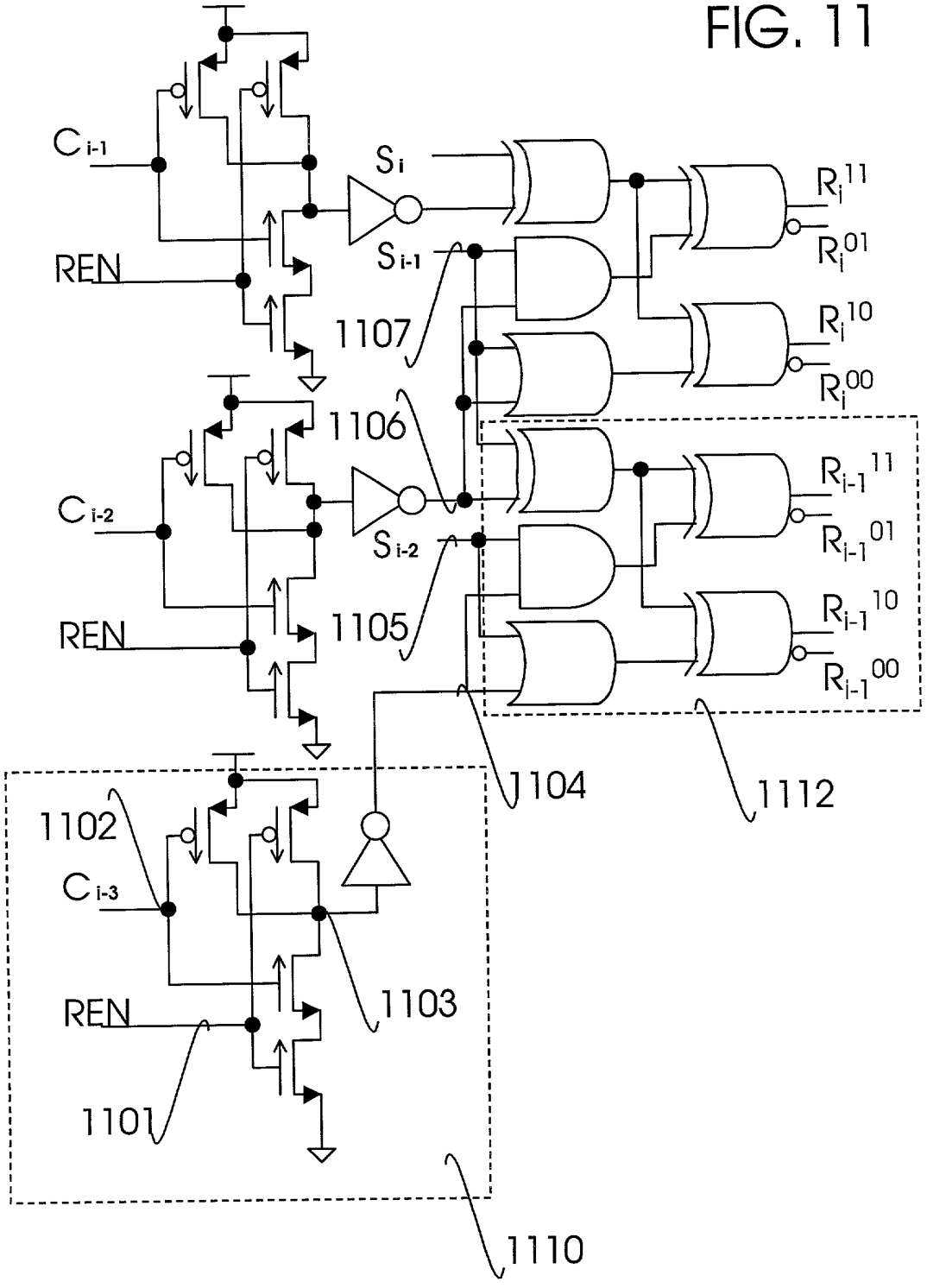

C i-1
REN
Si
Si-1
1107
1106
C i-2
REN
Si-2
1105
1104
1112
1102
C i-3
REN
1103
1101
1110
Ri 11
Ri 01
Ri 10
Ri 00
Ri-1 11
Ri-1 01
Ri-1 10
Ri-1 00

FIG. 12

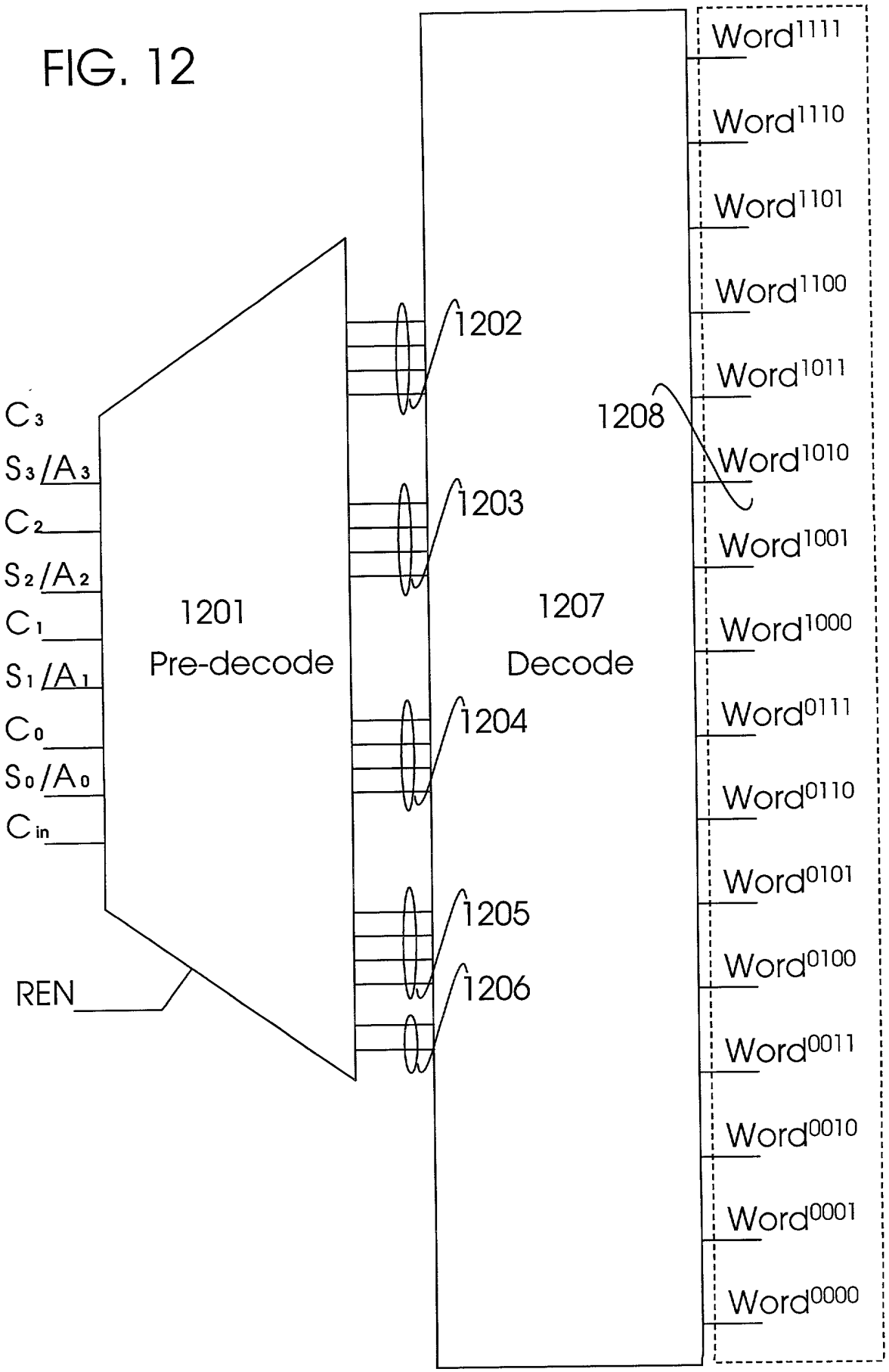

C3
S3/A3
C2
S2/A2
C1
S1/A1
C0
S0/A0
Cin
REN
1201
Pre-decode
1202
1203
1204
1205
1206
1207
Decode
1208
Word1111
Word1110
Word1101
Word1100
Word1011
Word1010
Word1001
Word1000
Word0111
Word0110
Word0101
Word0100
Word0011
Word0010
Word0001
Word0000

FIG. 13a

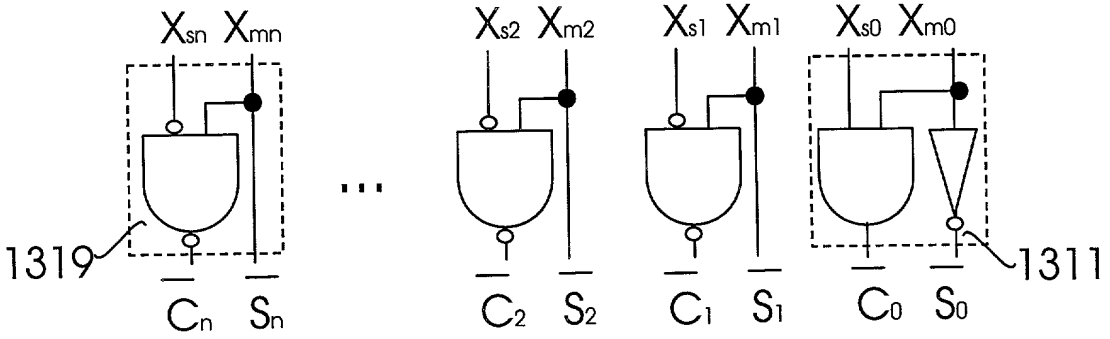


FIG. 13b

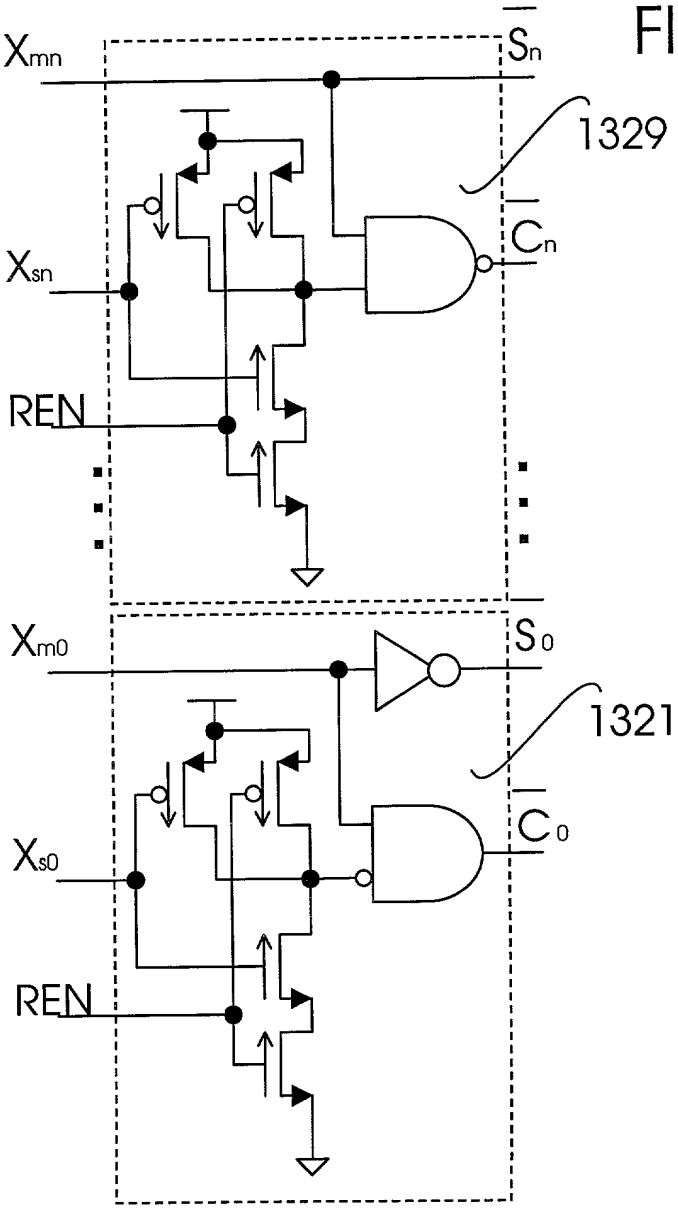


FIG. 14

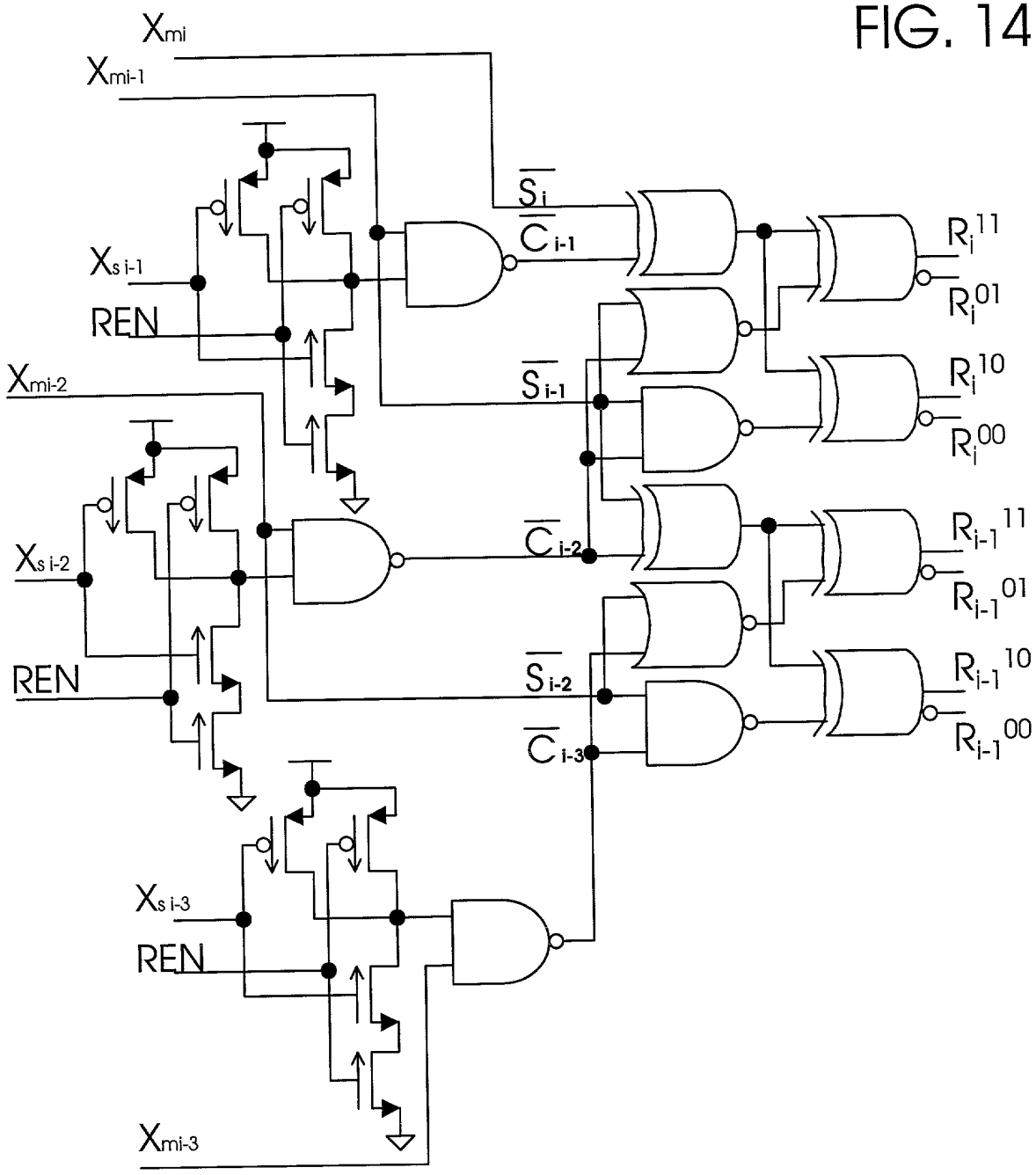

Xmi
Xmi-1
Xs i-1
REN
Xmi-2
Xs i-2
REN
Xs i-3
REN
Xmi-3
Si
Ci-1
Si-1
Ci-2
Si-2
Ci-3
Ri11
Ri01
Ri10
Ri00
Ri-111
Ri-101
Ri-110
Ri-100

FIG. 15

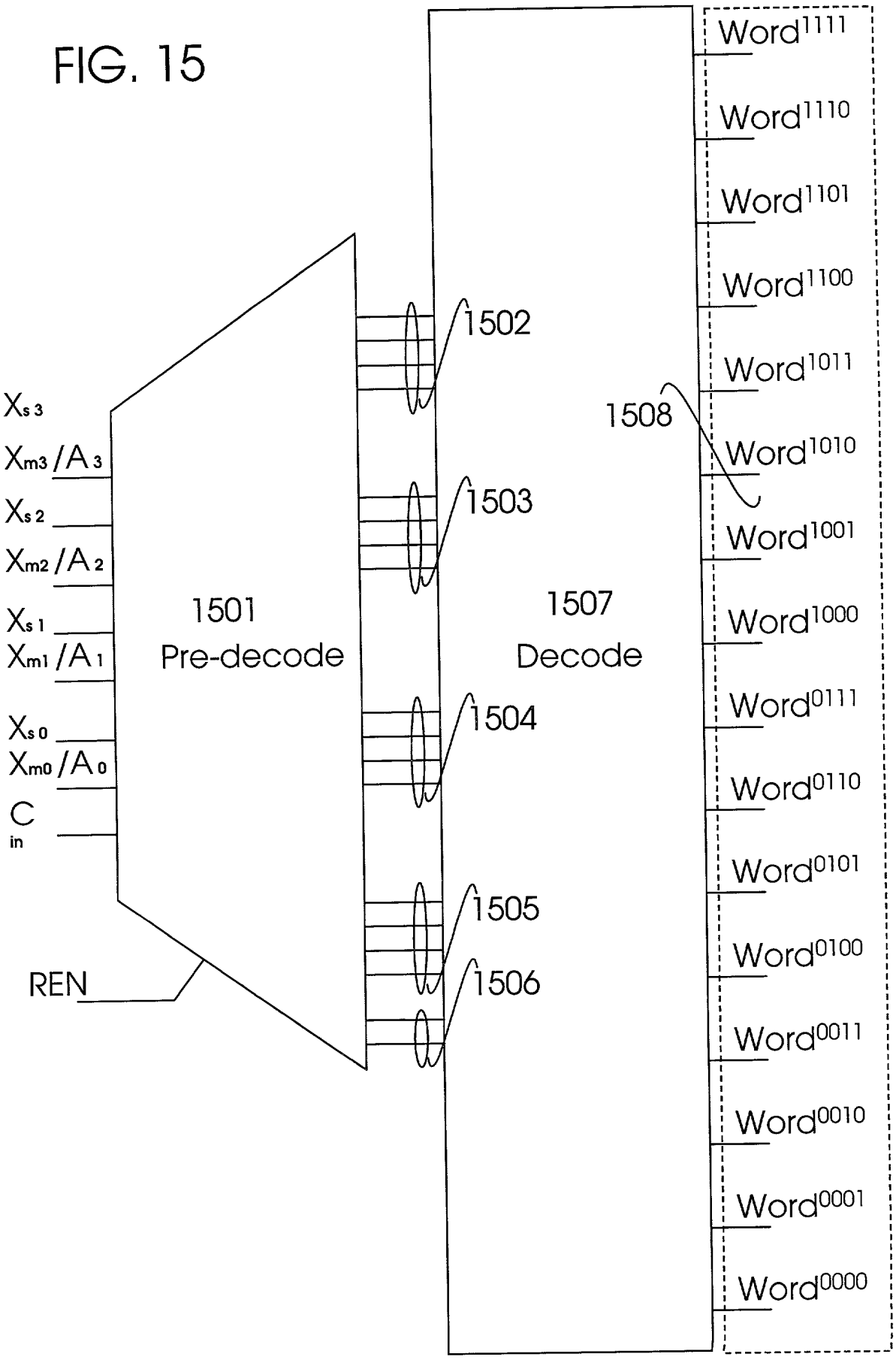

Word1111
Word1110
Word1101
Word1100
Word1011
Word1010
Word1001
Word1000
Word0111
Word0110
Word0101
Word0100
Word0011
Word0010
Word0001
Word0000
1502
1503
1504
1505
1506
1508
1501
Pre-decode
1507
Decode
Xs3
Xm3/A3
Xs2
Xm2/A2
Xs1
Xm1/A1
Xs0
Xm0/A0
Cin
REN

FIG. 16

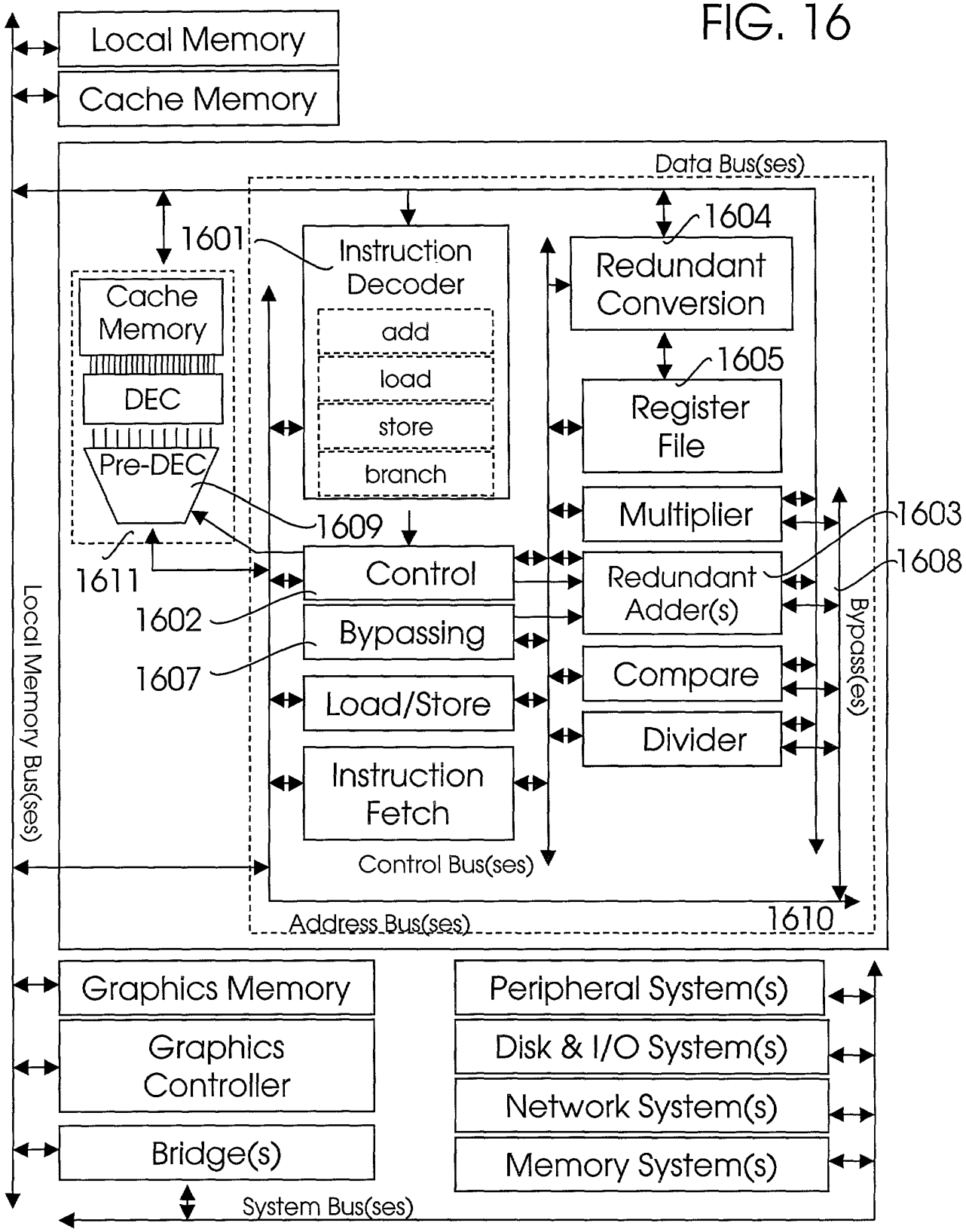
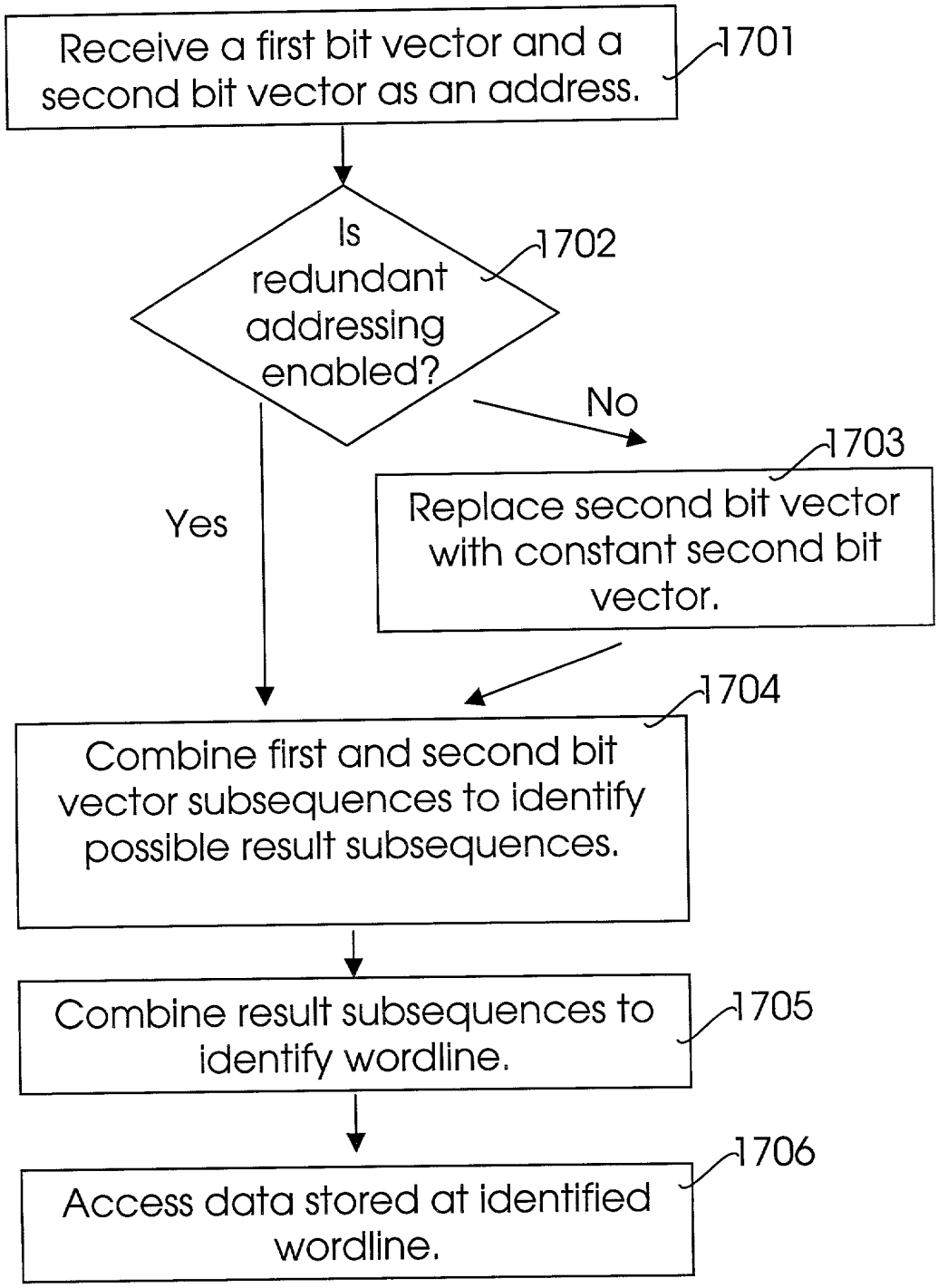

Local Memory
Cache Memory
Data Bus(ses)
1601
Instruction Decoder
add
load
store
branch
1604
Redundant Conversion
1605
Register File
Cache Memory
DEC
Pre-DEC
1609
Multiplier
1603
1608
1611
Control
Redundant Adder(s)
1602
Bypassing
1607
Compare
Load/Store
Divider
Instruction Fetch
Bypass(es)
Local Memory Bus(ses)
Control Bus(ses)
Address Bus(ses)
1610
Graphics Memory
Graphics Controller
Bridge(s)
Peripheral System(s)
Disk & I/O System(s)
Network System(s)
Memory System(s)
System Bus(ses)

FIG. 17


Receive a first bit vector and a second bit vector as an address.
1701
Is redundant addressing enabled?
1702
No
Yes
1703
Replace second bit vector with constant second bit vector.
1704
Combine first and second bit vector subsequences to identify possible result subsequences.
Combine result subsequences to identify wordline.
1705
Access data stored at identified wordline.
1706

Attorney's Docket No.: 42390.P8265 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
"SHARED CACHE WOKDLINE DECODER FOR REDUNDANT AND REGULAR ADDRESSES"

the specification of which

X is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Michael J. Mallie, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Michael J. Mallie, (408) 720-8300.
(Name of Attorney or Agent)
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Kevin X. Zhang

Inventor's Signature _____ Date _____

Residence Portland, Oregon (City, State) Citizenship P.R. China (Country)

Post Office Address 14258 NW Tradewind St.
Portland, Oregon 97229

Full Name of Second/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

Full Name of Third/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.